查询CY62128V供应商

CY62128V Family

128K x 8 Static RAM

Features

- **Low voltage range:**
  - **— 2.7V–3.6V (CY62128V)**
  - **— 2.3V–2.7V (CY62128V25)**
  - **— 1.6V–2.0V (CY62128V18)**
- **Low active power and standby power**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

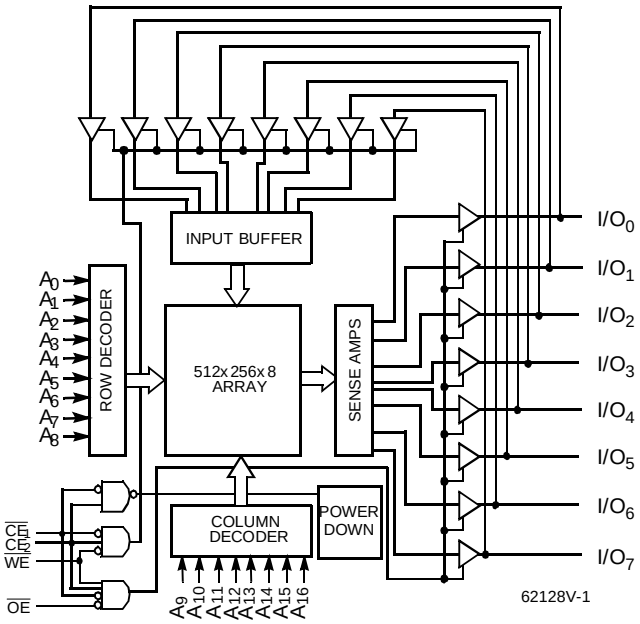
The CY62128V family is composed of three high-performance CMOS static RAMs organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE_1}$), an active HIGH Chip Enable (CE_2), an active LOW Output Enable ($\overline{OE}$) and three-state drivers. These devices have an automatic power-down feature, reducing the power consumption by over 99% when deselected. The CY62128V family is available in the standard 450-mil-wide SOIC, 32-lead TSOP-I, and STSOP packages.

Writing to the device is accomplished by taking Chip Enable one ($\overline{CE_1}$) and Write Enable ($\overline{WE}$) inputs LOW and the Chip Enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable one ($\overline{CE_1}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) and Chip Enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE_1}$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE_1}$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

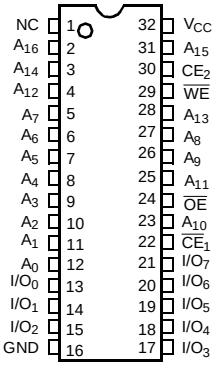
Logic Block Diagram



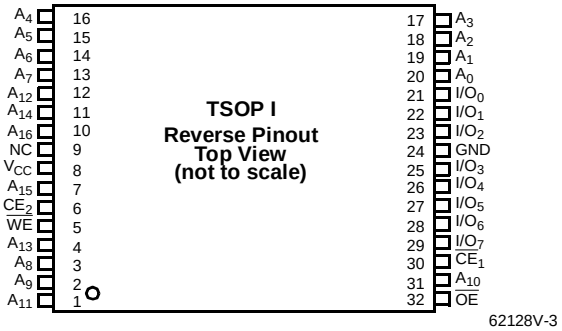
62128V-1

Pin Configurations

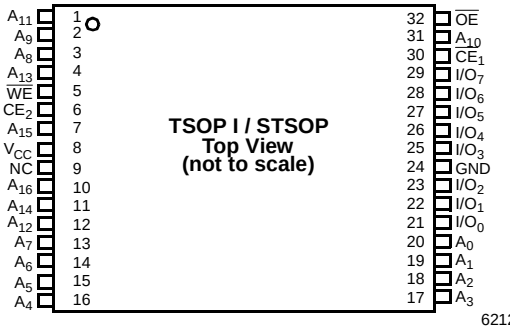
Top View
SOIC



62128V-2



62128V-3



62128V-4

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[1]..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[1]..... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	1.6V to 3.6V
Industrial	–40°C to +85°C	1.6V to 3.6V

Product Portfolio

Product	V_{CC} Range			Speed	Power Dissipation (Commercial)			
					Operating (I_{CC})		Standby (I_{SB2})	
	Min.	Typ.[2]	Max.		Typ.[2]	Maximum	Typ.[2]	Maximum
CY62128V	2.7V	3.0V	3.6V	55, 70 ns	20 mA	40 mA	0.4 µA	100 µA (XL = 10 µA)
CY62128V25	2.3V	2.5V	2.7V	100 ns	15 mA	20 mA	0.3 µA	50 µA (LL = 12 µA)
CY62128V18	1.6V	1.8V	2.0V	200 ns	10 mA	15 mA	0.3 µA	30 µA (LL = 10 µA)

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			CY62128V-55/70			Unit
					Min.	Typ.[2]	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA					0.4	V
V_{IH}	Input HIGH Voltage				2		V_{CC} +0.5V	V
V_{IL}	Input LOW Voltage				–0.5		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			–1	±1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			–1	±1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l, 70 ns	L		20	40	mA
				LL, XL		20	40	
			Ind'l, 55 ns	LL		23	50	
			Ind'l, 70 ns	L		20	40	
				LL		20	40	
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l, 70 ns	L		15	300	µA
				LL, XL		15	300	
			Coml, 55 ns	LL		17	350	
			Ind'l	L		15	300	
				LL		15	300	

Notes:
1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ., T_A = 25°C.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			CY62128V-55/70 Min.	CY62128V-55/70 Typ.[2]	CY62128V-55/70 Max.	Unit
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, f = 0	Com'l	L		0.4	100	µA
				LL			15	µA
				XL			10	µA
			Ind'l	L			100	µA
				LL			30	µA

Electrical Characteristics Over the Operating Range

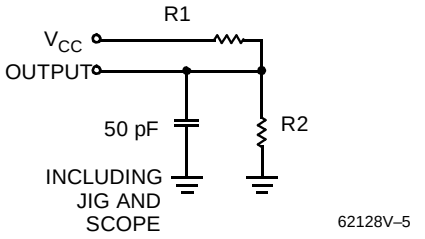
Parameter	Description	Test Conditions		CY62128V25-100 Min.	CY62128V25-100 Typ.[2]	CY62128V25-100 Max.	CY62128V18-200 Min.	CY62128V18-200 Typ.[2]	CY62128V18-200 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –0.1 mA		2.4			0.8* V_{CC}			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 0.1 mA				0.4			0.2	V
V_{IH}	Input HIGH Voltage			2		V_{CC} +0.5	0.7* V_{CC}		V_{CC} +0.3	V
V_{IL}	Input LOW Voltage			–0.5		0.8	–0.5		0.3* V_{CC}	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	±1	+1	–1	±0.1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1	±1	+1	–1	±0.1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	L		15	20		10	15	mA
			LL							
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	L		15	300		5	100	µA
			LL							
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, f = 0	L		0.4	50		0.4	30	µA
			LL			12			10	µA
		Indust'l Temp Range	LL			24			20	µA

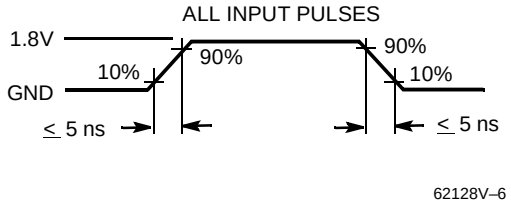
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.0V	6	pF
C_{OUT}	Output Capacitance		8	pF

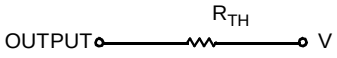
Note:
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT

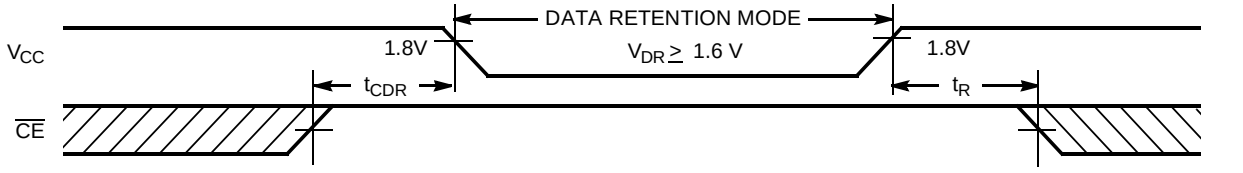


Parameters	3.3V	2.5V	1.8V	Unit
R1	1213	15909	10800	Ohms
R2	1378	4487	4154	Ohms
R_{TH}	645	3500	3000	Ohms
V_{TH}	1.75V	0.55V	0.50V	Volts

Data Retention Characteristics (Over the Operating Range)

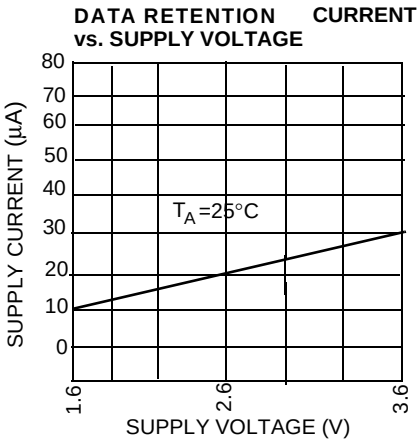
Parameter	Description			Conditions[4]	Min.	Typ.[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention				1.6			V
I_{CCDR}	Data Retention Current	Com'l	L	V_{CC} = 2V $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ No input may exceed V_{CC}+0.3V		0.4	10	µA
			LL, XL				10	µA
		Ind'l	L				20	µA
			LL				20	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time				0			ns
t_R	Operation Recovery Time				t_{RC}			ns

Data Retention Waveform



Note:
4. No input may exceed V_{CC}+0.3V.

Data Retention Current Graph (for “L” version only)



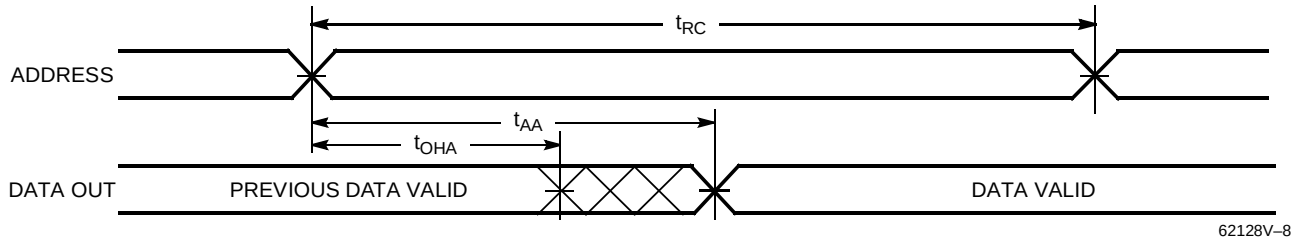
Switching Characteristics Over the Operating Range[5]

Parameter	Description	62128V-55		62128V-70		62128V25-100		62128V18-200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	55		70		100		200		ns
t_{AA}	Address to Data Valid		55		70		100		200	ns
t_{OHA}	Data Hold from Address Change	5		10		10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		55		70		100		200	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		20		35		75		125	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6]	10		10		10		10		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		20		25		50		75	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	10		10		10		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		20		25		50		75	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		55		70		100		200	ns
WRITE CYCLE[8, 9]										
t_{WC}	Write Cycle Time	55		70		100		200		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	45		60		100		190		ns
t_{AW}	Address Set-Up to Write End	45		60		100		190		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	45		55		90		125		ns
t_{SD}	Data Set-Up to Write End	25		30		60		100		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		20		25		50		100	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	5		5		10		15		ns

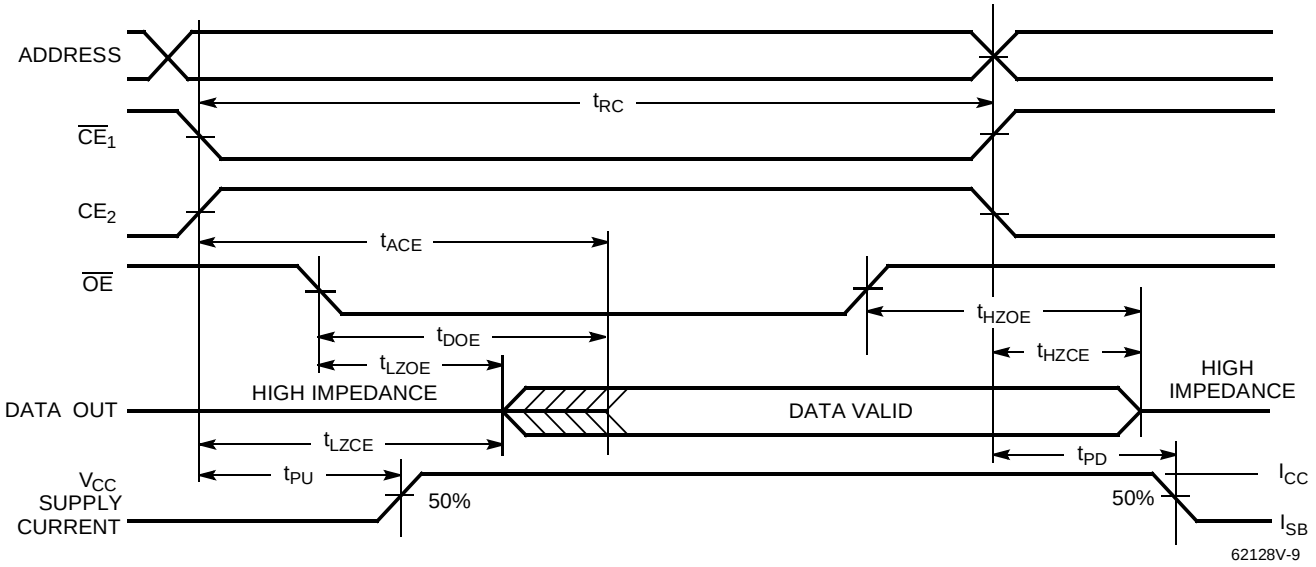
5. Test conditions assume signal transition time of 5 ns or less timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ signals must be LOW and CE_2 HIGH to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

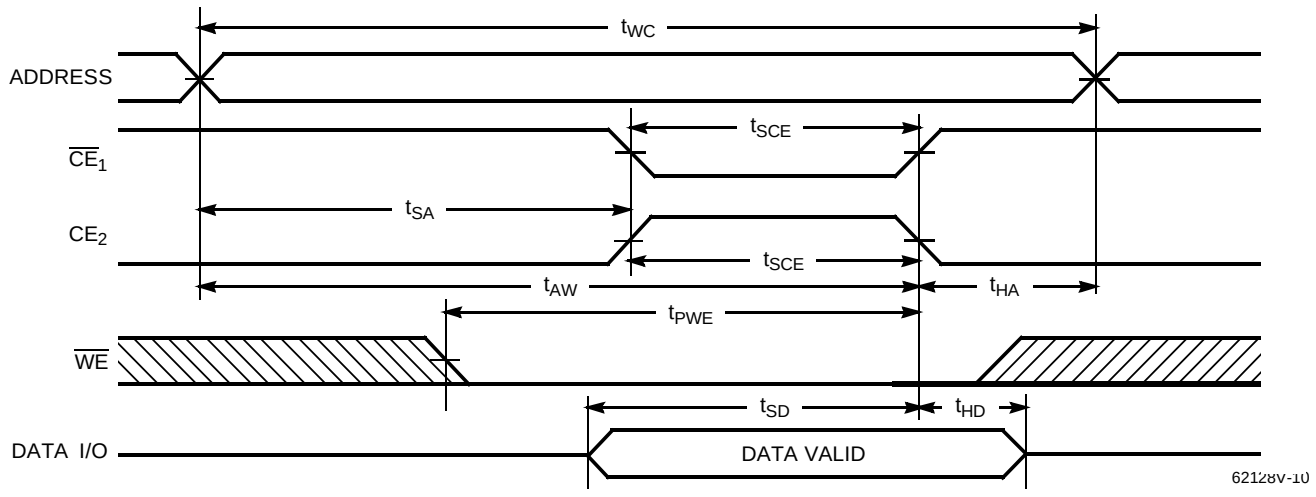
Read Cycle No. 1[10, 11]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[11, 12]



Write Cycle No. 1 ($\overline{CE_1}$ or CE_2 Controlled)[13,14]

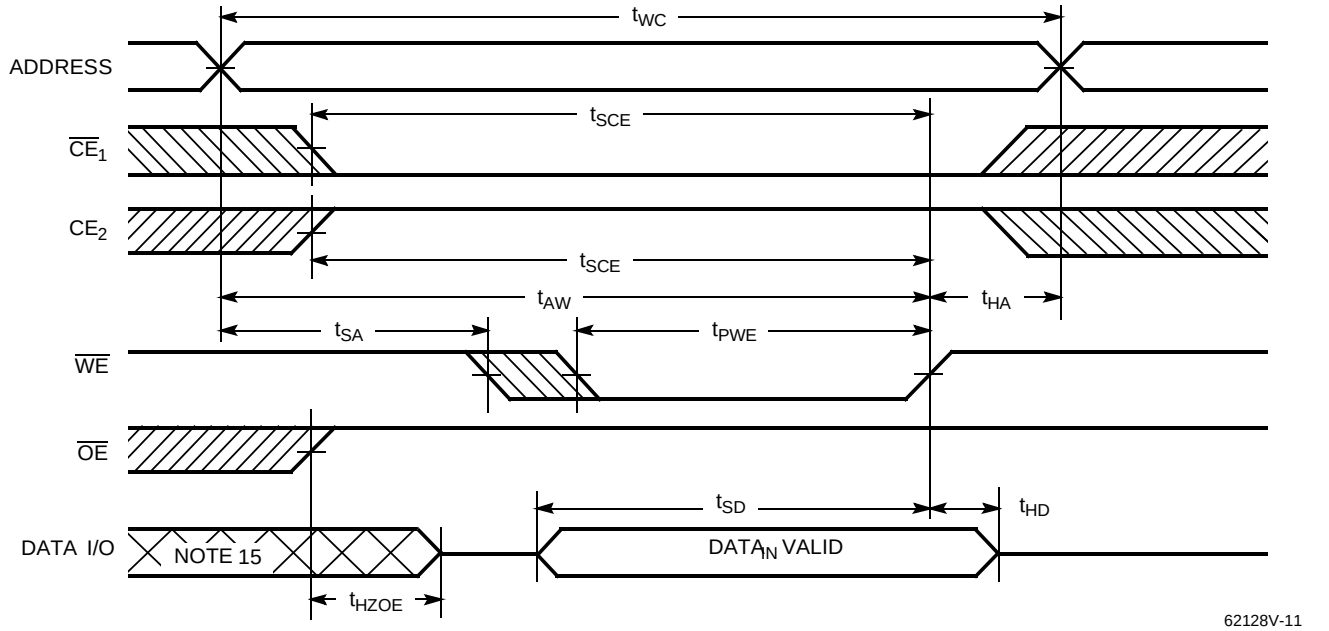


Notes:

10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, CE_2=V_{IH}.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.
13. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
14. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[13, 14]



Note:
15. During this period, the I/Os are in output state and input signals should not be applied.

Truth Table

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62128VLL-55ZAI	ZA32	32-Lead STSOP Type 1	Industrial
70	CY62128VL-70SC	S34	32-Lead 450-Mil SOIC	Commercial
	CY62128VLL-70SC	S34		
	CY62128VL-70ZC	Z32	32-Lead TSOP Type 1	
	CY62128VLL-70ZC	Z32		
	CY62128VXL-70ZC	Z32		
	CY62128VL-70ZAC	ZA32	32-Lead STSOP Type 1	
	CY62128VLL-70ZAC	ZA32		
	CY62128VL-70ZRC	ZR32	32-Lead Reverse TSOP 1	
	CY62128VLL-70ZRC	ZR32		
70	CY62128VL-70SI	S34	32-Lead 450-Mil SOIC	Industrial
	CY62128VLL-70SI	S34		
	CY62128VL-70ZI	Z32	32-Lead TSOP Type 1	
	CY62128VLL-70ZI	Z32		
	CY62128VL-70ZAI	ZA32	32-Lead STSOP Type 1	
	CY62128VLL-70ZAI	ZA32		
	CY62128VL-70ZRI	ZR32	32-Lead Reverse TSOP 1	
	CY62128VLL-70ZRI	ZR32		
100	CY62128V25L-100SC	S34	32-Lead 450-Mil SOIC	Commercial
	CY62128V25LL-100SC	S34		
	CY62128V25L-100ZC	Z32	32-Lead TSOP Type 1	
	CY62128V25LL-100ZC	Z32		
	CY62128V25L-100ZAC	ZA32	32-Lead STSOP Type 1	
	CY62128V25LL-100ZAC	ZA32		
	CY62128V25L-100ZRC	ZR32	32-Lead Reverse TSOP 1	
	CY62128V25LL-100ZRC	ZR32		
100	CY62128V25L-100SI	S34	32-Lead 450-Mil SOIC	Industrial
	CY62128V25LL-100SI	S34		
	CY62128V25L-100ZI	Z32	32-Lead TSOP Type 1	
	CY62128V25LL-100ZI	Z32		
	CY62128V25L-100ZAI	ZA32	32-Lead STSOP Type 1	
	CY62128V25LL-100ZAI	ZA32		
	CY62128V25L-100ZRI	ZR32	32-Lead Reverse TSOP 1	
	CY62128V25LL-100ZRI	ZR32		
200	CY62128V18L-200SC	S34	32-Lead 450-Mil SOIC	Commercial
	CY62128V18LL-200SC	S34		
	CY62128V18L-200ZC	Z32	32-Lead TSOP Type 1	
	CY62128V18LL-200ZC	Z32		
	CY62128V18L-200ZAC	ZA32	32-Lead STSOP Type 1	
	CY62128V18LL-200ZAC	ZA32		
	CY62128V18L-200ZRC	ZR32	32-Lead Reverse TSOP 1	
	CY62128V18LL-200ZRC	ZR32		

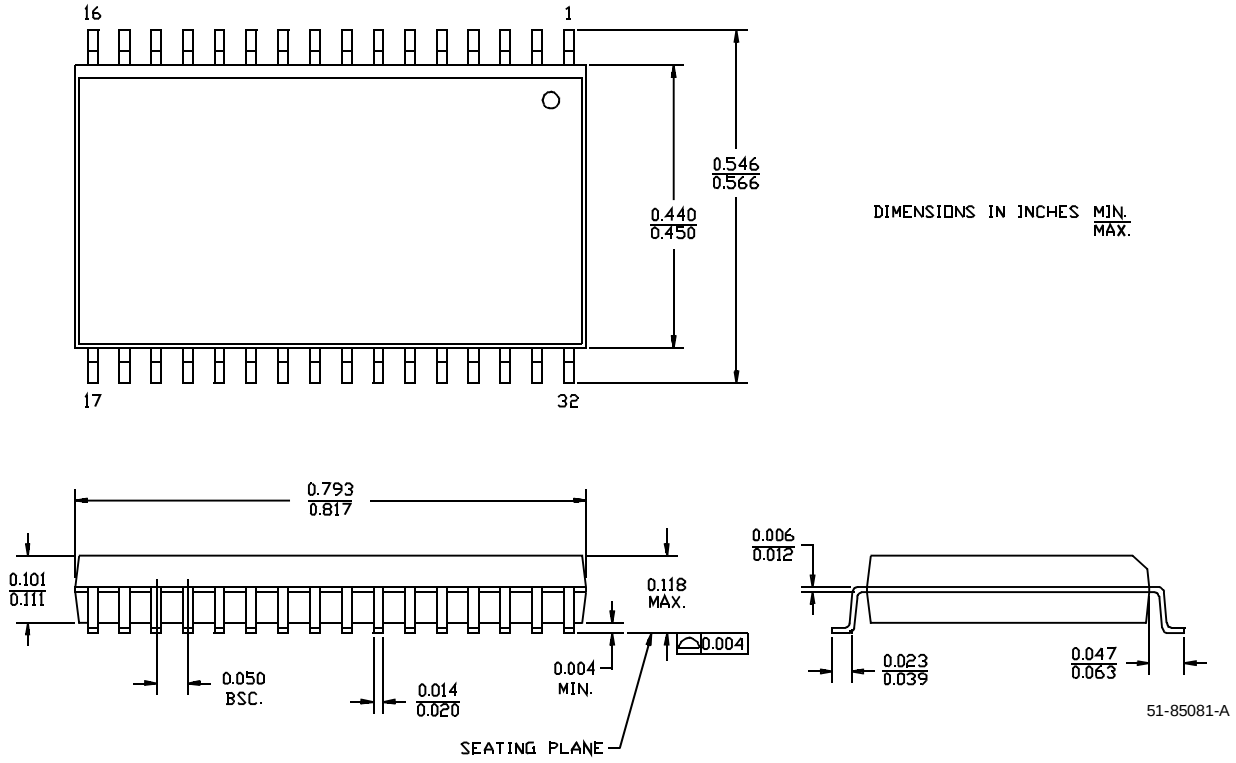
Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
200	CY62128V18L-200SI	S34	32-Lead 450-Mil SOIC	Industrial
	CY62128V18LL-200SI	S34		
	CY62128V18L-200ZI	Z32	32-Lead TSOP Type 1	
	CY62128V18LL-200ZI	Z32		
	CY62128V18L-200ZAI	ZA32	32-Lead STSOP Type 1	
	CY62128V18LL-200ZAI	ZA32		
	CY62128V18L-200ZRI	ZR32	32-Lead Reverse TSOP 1	
	CY62128V18LL-200ZRI	ZR32		

Document #: 38-00547-B

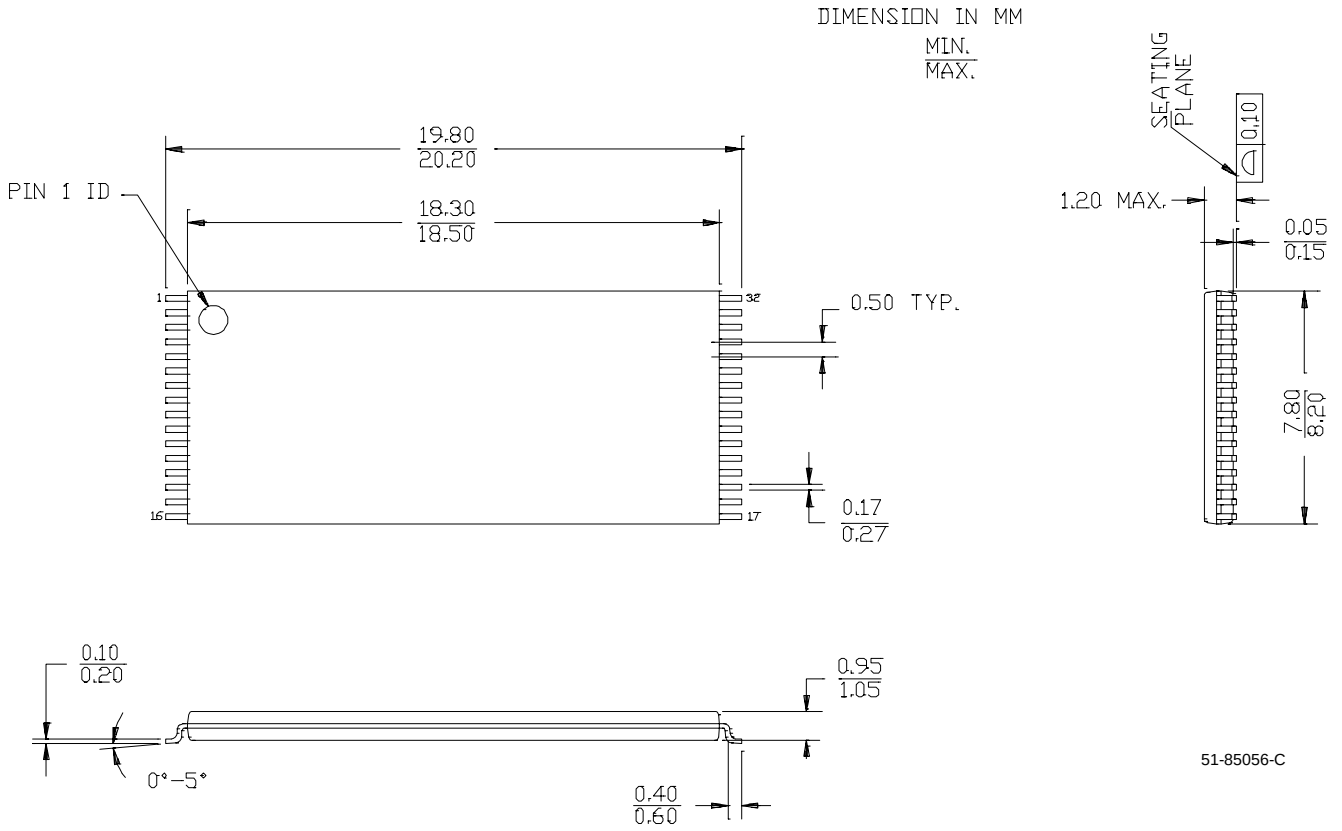
Package Diagrams

32-Lead (450 MIL) Molded SOIC S34



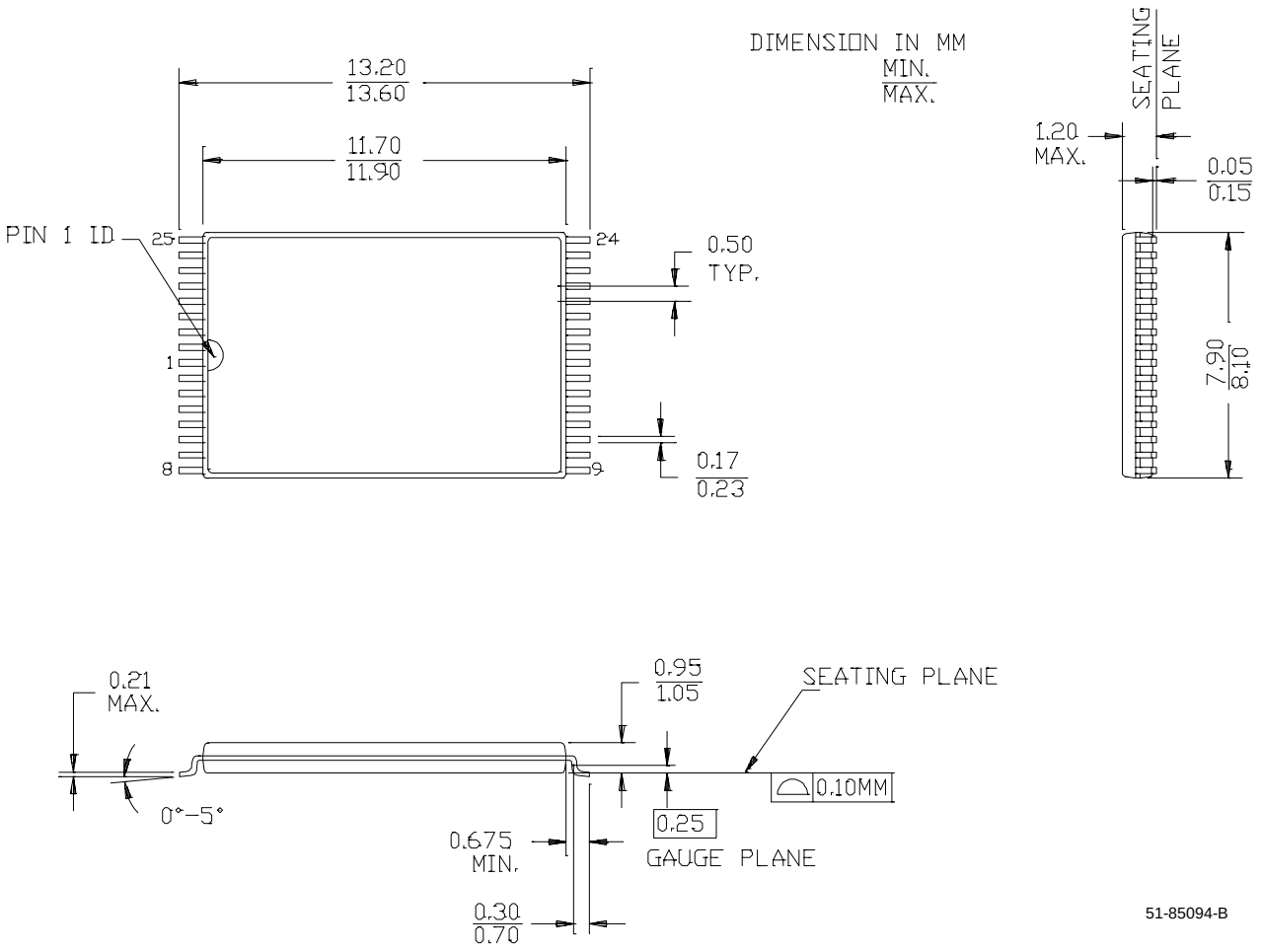
Package Diagrams (continued)

32-Lead Thin Small Outline Package Z32



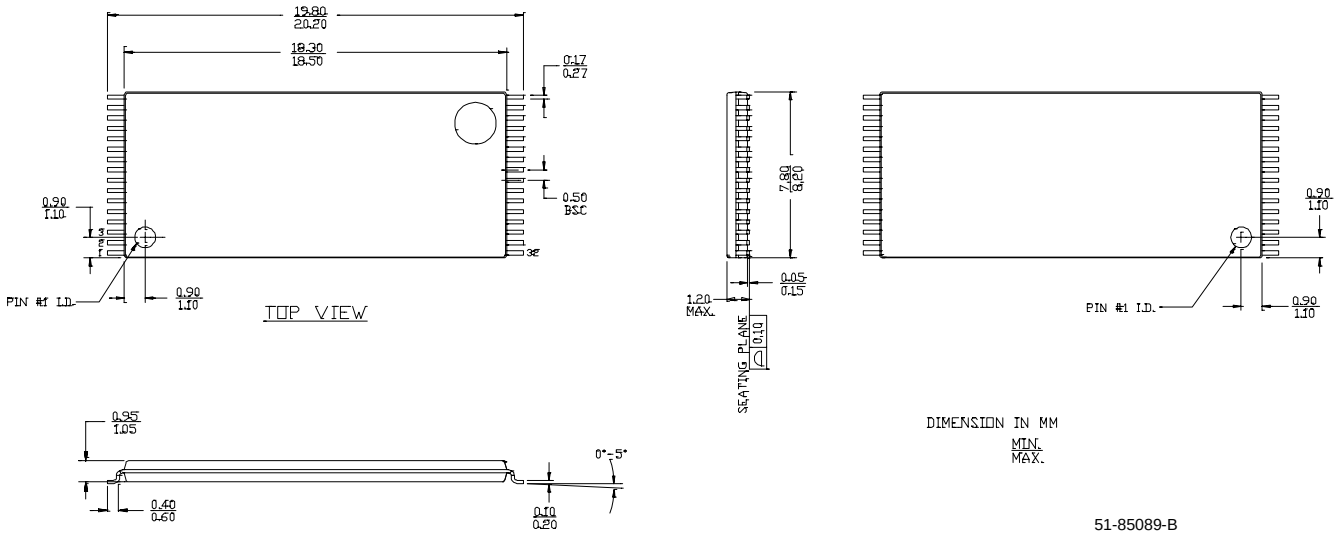
Package Diagrams (continued)

32-Lead Shrunk Thin Small Outline Package ZA32



Package Diagrams (continued)

32-Lead Reverse Thin Small Outline Package ZR32



© Cypress Semiconductor Corporation, 2000. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress Semiconductor product. Nor does it convey or imply any license under patent or other rights. Cypress Semiconductor does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress Semiconductor products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress Semiconductor against all charges.